Parallel VHDL Simulation

Charm++

- Charm++ is a runtime system which can be used by parallel programs.
- Works with Charm++ communication library (communication optimization).
- Periodically checkpoints processors during execution.
- Keeps track of simulation time.
- What does POSE add?

POSE

- Translates Charm++ to C++.
- Generates processor tick for each cycle.
- AVD files are used to manage tick.

ONE CU: 1000 ticks = 500000 instruction cycles

VHDL - Basic Overview

- VHDL stands for "Very High Speed Integrated Circuits Hardware Description Language".
- It is a high-level programming language used to describe digital systems.
- It is supported by a popular free tool called Xilinx ISE or Altera Quartus.

VHDL File

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOT, GATE</td>
<td>Process data with 0 or 1, inverting input</td>
</tr>
<tr>
<td>and, OR, GATE</td>
<td>Process data with 0 or 1, combining inputs</td>
</tr>
<tr>
<td>nand, nOR, GATE</td>
<td>Process data with 0 or 1, combining inputs with negation</td>
</tr>
<tr>
<td>NAND, NANDGATE, OR, ORGATE</td>
<td>Process data with 0 or 1, combining inputs and outputs</td>
</tr>
</tbody>
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VHDL Simulator

- The VHDL code is translated into a series of C++ files.
- Each entity declaration is translated into a C++ class with the same name.
- Each signal is translated into a C++ variable.
- Each component is translated into a C++ function.

VHDL Translator

- VHDL is first parsed and then translated into a C++ program.
- The C++ code is then compiled and executed.

Simulation Overview

- After the VHDL code has been compiled and linked, the executable can be run
- The VHDL code is executed as a series of C++ functions.
- The output of each component is stored in a file.

VHDL Support So Far

- Translator: Charm++, POSE, & Parallel Processing Lab (PPL)
- Simulation: VCDGenerator
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- Simulation: VCDGenerator

Initial Results

- The above graph shows the performance of the Charm++/POSE simulator on a single processor.
- The graph shows the time taken for different components to execute.
- The performance of the simulator is measured in terms of execution time.

Another POSE Related Project: BigNetSim

- BigNetSim is a tool for simulating large-scale parallel systems.
- It allows for the simulation of thousands of processors in a single model.
- The simulation can be used to study the behavior of parallel systems under various conditions.

Future Work

- Create strategies specifically designed to accommodate the behavior of components and VCDGenerator.
- Support for other HDL languages (specifically, the VHDL language).
- Further development of shared virtual machines for the VCDGenerator framework.

For More Information, Please Visit the PPL Website: http://charm.cs.uiuc.edu